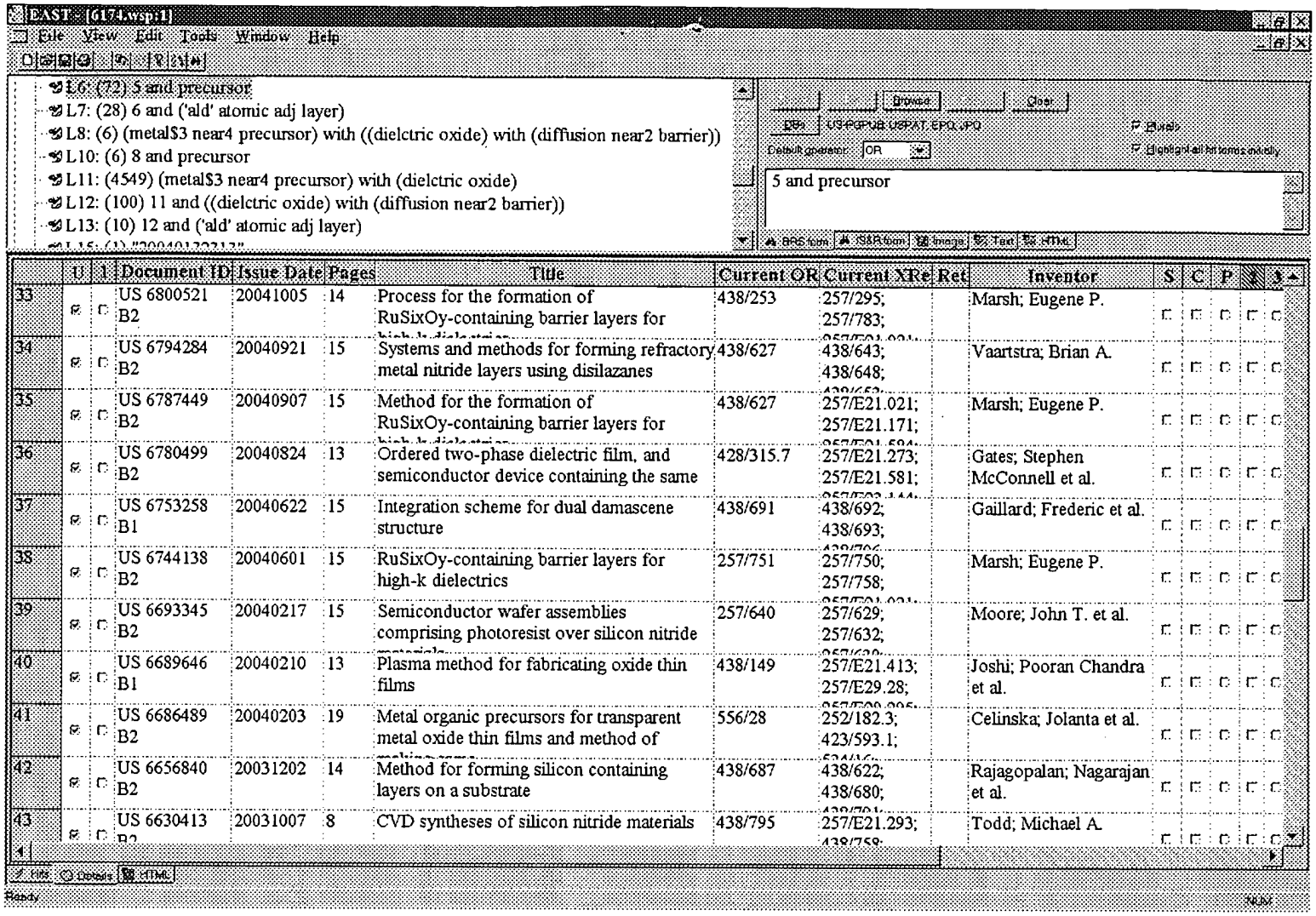
Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
		(metal$3 near4 precursor) with ((dielctric oxide)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 10:46
		("(microadjstructuremicrostructure)with(gripermanipulator)").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/11/30 13:36
L1	1935	(oxide near4 (aluminum tatalum titanium)) with precursor	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 09:17
L2	1269	((silicon germanium) near2 containing) with precursor	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 09:25
L3	2493	(diffusi$3 near2 barrier) with (dielectric)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 09:35
L4	4100	(diffusi$3 near2 barrier) with (dielectric oxide)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 09:35
L5	72	2 and 4	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 09:40
L6	72	5 and precursor	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 13:08
L7	28	6 and ('ald' atomic adj layer)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 10:46
L8	6	(metal$3 near4 precursor) with ((dielctric oxide) with (diffusion near2 barrier))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 10:46
L9	72	6 and precursor	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 14:23
L10	6	8 and precursor	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 10:37
L11	4549	(metal$3 near4 precursor) with (dielctric oxide)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 10:46

L12	100	11 and ((dielctric oxide) with (diffusion near2 barrier))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 10:46
L13	10	12 and ('ald' atomic adj layer)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 10:52
L14	10	12 and (atomic adj layer)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 13:15
L15	1	"20040132313"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 13:08
L16	15	"6077774"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 14:39
L17	2	10/215990	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 15:22
L18	73	"6203613"	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 15:25
L19	2	10/215990	US-PGPUB; USPAT; EPO; JPO	OR	ON	2005/01/04 15:25
S1	71993	(method process$3) with (side adj wall sidewall spacer)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/06/06 10:43
S2	10472	((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:43
S3	8483	(((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and ((etch$3) with (side adj wall sidewall spacer))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:44
S4	3612	(((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 08:42

S5	1636	((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45
S6	1636	(((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidwall spacer side wall plasma vapor etching etch$2 gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45
S7	364	((((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidwall spacer side wall plasma vapor etching etch$2 gate)) and ((rotation$2 rotat$2 rotating spin$4 turning turn$3) with substrate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 08:50

S8	99	((((((method process$3) with (side adj wall sidewall spacer)) and ((substrate with gate) same (dielectric oxide))) and (etch$3 with (plasma vapor))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidwall spacer side wall plasma vapor etching etch$2 gate)) and ((rotation$2 rotat$2 rotating spin$4 turning turn$3) with substrate)) and (acid with etch$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 08:51
S9	10135	(method process$3) with ((side adj wall sidewall spacer) with (gate transistor))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:41
S10	28954	((side adj wall sidewall spacer) with (gate transistor))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:43
S11	22184	(((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:44
S12	13851	((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:45
S13	4977	(((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))) and (substrate with (anneal$3 heat$3 themal$5 temperature))	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:46

S14	4977	((((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidewall spacer side wall plasma vapor etching etch$2 gate insulat$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:48
S15	2079	(((((((side adj wall sidewall spacer) with (gate transistor))) and ((dielectric insulat$3 oxide) with gate)) and ((etch$3) with (side adj wall$1 sidewall$1 spacer$1))) and (substrate with (anneal$3 heat$3 themal$5 temperature))) and (substrate anneal$3 heat$3 themal$5 temperature gate dielectric oxide sidewall spacer side wall plasma vapor etching etch$2 gate insulat$3)) and (wet near5 etch$3)	US-PGPUB; USPAT; EPO; JPO	OR	ON	2003/05/27 09:48



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRe	Ret	Inventor	S	C	P	2	3
33	☑	☐	US 6800521 B2	20041005	14	Process for the formation of RuSixOy-containing barrier layers for	438/253	257/295; 257/783;		Marsh; Eugene P.	☐	☐	☐	☐	☐
34	☑	☐	US 6794284 B2	20040921	15	Systems and methods for forming refractory metal nitride layers using disilazanes	438/627	438/643; 438/648;		Vaartstra; Brian A.	☐	☐	☐	☐	☐
35	☑	☐	US 6787449 B2	20040907	15	Method for the formation of RuSixOy-containing barrier layers for	438/627	257/E21.021; 257/E21.171;		Marsh; Eugene P.	☐	☐	☐	☐	☐
36	☑	☐	US 6780499 B2	20040824	13	Ordered two-phase dielectric film, and semiconductor device containing the same	428/315.7	257/E21.273; 257/E21.581;		Gates; Stephen McConnell et al.	☐	☐	☐	☐	☐
37	☑	☐	US 6753258 B1	20040622	15	Integration scheme for dual damascene structure	438/691	438/692; 438/693;		Gaillard; Frederic et al.	☐	☐	☐	☐	☐
38	☑	☐	US 6744138 B2	20040601	15	RuSixOy-containing barrier layers for high-k dielectrics	257/751	257/750; 257/758;		Marsh; Eugene P.	☐	☐	☐	☐	☐
39	☑	☐	US 6693345 B2	20040217	15	Semiconductor wafer assemblies comprising photoresist over silicon nitride	257/640	257/629; 257/632;		Moore; John T. et al.	☐	☐	☐	☐	☐
40	☑	☐	US 6689646 B1	20040210	13	Plasma method for fabricating oxide thin films	438/149	257/E21.413; 257/E29.28;		Joshi; Pooran Chandra et al.	☐	☐	☐	☐	☐
41	☑	☐	US 6686489 B2	20040203	19	Metal organic precursors for transparent metal oxide thin films and method of	556/28	252/182.3; 423/593.1;		Celinska; Jolanta et al.	☐	☐	☐	☐	☐
42	☑	☐	US 6656840 B2	20031202	14	Method for forming silicon containing layers on a substrate	438/687	438/622; 438/680;		Rajagopalan; Nagarajan et al.	☐	☐	☐	☐	☐
43	☑	☐	US 6630413 B2	20031007	8	CVD syntheses of silicon nitride materials	438/795	257/E21.293;		Todd; Michael A.	☐	☐	☐	☐	☐

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L6: (72) 5 and precursor
L7: (28) 6 and ('ald' atomic adj layer)
L8: (6) (metal$3 near4 precursor) with ((dielctric oxide) with (diffusion near2 barrier))
L10: (6) 8 and precursor
L11: (4549) (metal$3 near4 precursor) with (dielctric oxide)
L12: (100) 11 and ((dielctric oxide) with (diffusion near2 barrier))
L13: (10) 12 and ('ald' atomic adj layer)
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Bibliography Abstract Image Text HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRe	Ret	Inventor	S	C	P	2	3
44	☑	☐	US 6605549 B2	20030812	12	Method for improving nucleation and adhesion of CVD and ALD films deposited	438/758	257/E21.576; 257/E21.584;		Leu; Jihperng et al.	☐	☐	☐	☐	☐
45	☑	☐	US 6605502 B2	20030812	19	Isolation using an antireflective coating	438/225	257/E21.029; 257/E21.258;		Iyer; Ravi et al.	☐	☐	☐	☐	☐
46	☑	☐	US 6566281 B1	20030520	10	Nitrogen-rich barrier layer and structures formed	438/786	257/E21.269; 257/E21.639;		Buchanan; Douglas Andrew et al.	☐	☐	☐	☐	☐
47	☑	☐	US 6559070 B1	20030506	39	Mesoporous silica films with mobile ion gettering and accelerated processing	438/781	257/E21.273; 427/162;		Mandal; Robert P.	☐	☐	☐	☐	☐
48	☑	☐	US 6534404 B1	20030318	10	Method of depositing diffusion barrier for copper interconnect in integrated circuit	438/680	257/E21.17; 257/E21.584;		Danek; Michal et al.	☐	☐	☐	☐	☐
49	☑	☐	US 6495450 B1	20021217	19	Isolation using an antireflective coating	438/636	257/E21.029; 257/E21.258;		Iyer; Ravi et al.	☐	☐	☐	☐	☐
50	☑	☐	US 6433430 B1	20020813		Contact structure having a diffusion barrier	257/751	257/754; 257/763;		Sharan; Sujit et al.	☐	☐	☐	☐	☐
51	☑	☐	US 6423631 B1	20020723		Isolation using an antireflective coating	438/636	257/510; 257/E21.029;		Iyer; Ravi et al.	☐	☐	☐	☐	☐
52	☑	☐	US 6417559 B1	20020709		Semiconductor wafer assemblies comprising photoresist over silicon nitride	257/640	257/629; 257/632;		Moore; John T. et al.	☐	☐	☐	☐	☐
53	☑	☐	US 6376691 B1	20020423		Metal organic precursors for transparent metal oxide thin films and method of	556/28	252/182.3; 534/15;		Celinska; Jolanta et al.	☐	☐	☐	☐	☐
54	☑	☐	US 6284651 B1	20010904		Method for forming a contact having a diffusion barrier	438/649	257/E21.165;		Sharan; Sujit et al.	☐	☐	☐	☐	☐

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DBs US-PGPUB,USPAT,EPO,JPO Bursts

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Ref	Inventor	S	C	P	2	3
55	☑	☐	US 6235456 B1	20010522		Graded anti-reflective barrier films for ultra-fine lithography	430/512	257/437		Ibok; Effiong E.	☐	☐	☐	☐	☐
56	☑	☐	US 6197628 B1	20010306		Ruthenium silicide diffusion barrier layers and methods of forming same	438/238	257/486; 257/740;		Vaartstra; Brian A. et al.	☐	☐	☐	☐	☐
57	☑	☐	US 6174590 B1	20010116		Isolation using an antireflective coating	428/209	257/E21.029; 257/E21.258;		Iyer; Ravi et al.	☐	☐	☐	☐	☐
58	☑	☐	US 6171703 B1	20010109		Hermetic substrate coatings in an inert gas atmosphere	428/446	257/E21.502; 257/E23.118;		Haluska; Loren Andrew	☐	☐	☐	☐	☐
59	☑	☐	US 6121133 A	20000919		Isolation using an antireflective coating	438/636	257/E21.029; 257/E21.258;		Iyer; Ravi et al.	☐	☐	☐	☐	☐
60	☑	☐	US 6096640 A	20000801		Method of making a gate electrode stack with a diffusion barrier	438/652	257/E21.2; 257/E29.157;		Hu; Yongjun	☐	☐	☐	☐	☐
61	☑	☐	US 5962904 A	19991005		Gate electrode stack with diffusion barrier	257/412	257/751; 257/915;		Hu; Yongjun	☐	☐	☐	☐	☐
62	☑	☐	US 5563102 A	19961008		Method of sealing integrated circuits	438/614	257/E23.167; 438/702;		Michael; Keith W.	☐	☐	☐	☐	☐
63	☑	☐	US 5436029 A	19950725		Curing silicon hydride containing materials by exposure to nitrous oxide	427/126.2	257/E21.271; 257/E23.12;		Ballance; David S. et al.	☐	☐	☐	☐	☐
64	☑	☐	US 5380567 A	19950110		Hermetic coatings by heating hydrogen silsesquinoxane resin in an inert atmosphere	427/578	257/E21.502; 257/E23.118;		Haluska; Loren A.	☐	☐	☐	☐	☐
65	☑	☐	US 5318857 A	19940607		Low temperature ozonolysis of silicon and ceramic oxide precursor polymers to	428/552	257/E21.271; 257/E23.118;		Haluska; Loren A.	☐	☐	☐	☐	☐

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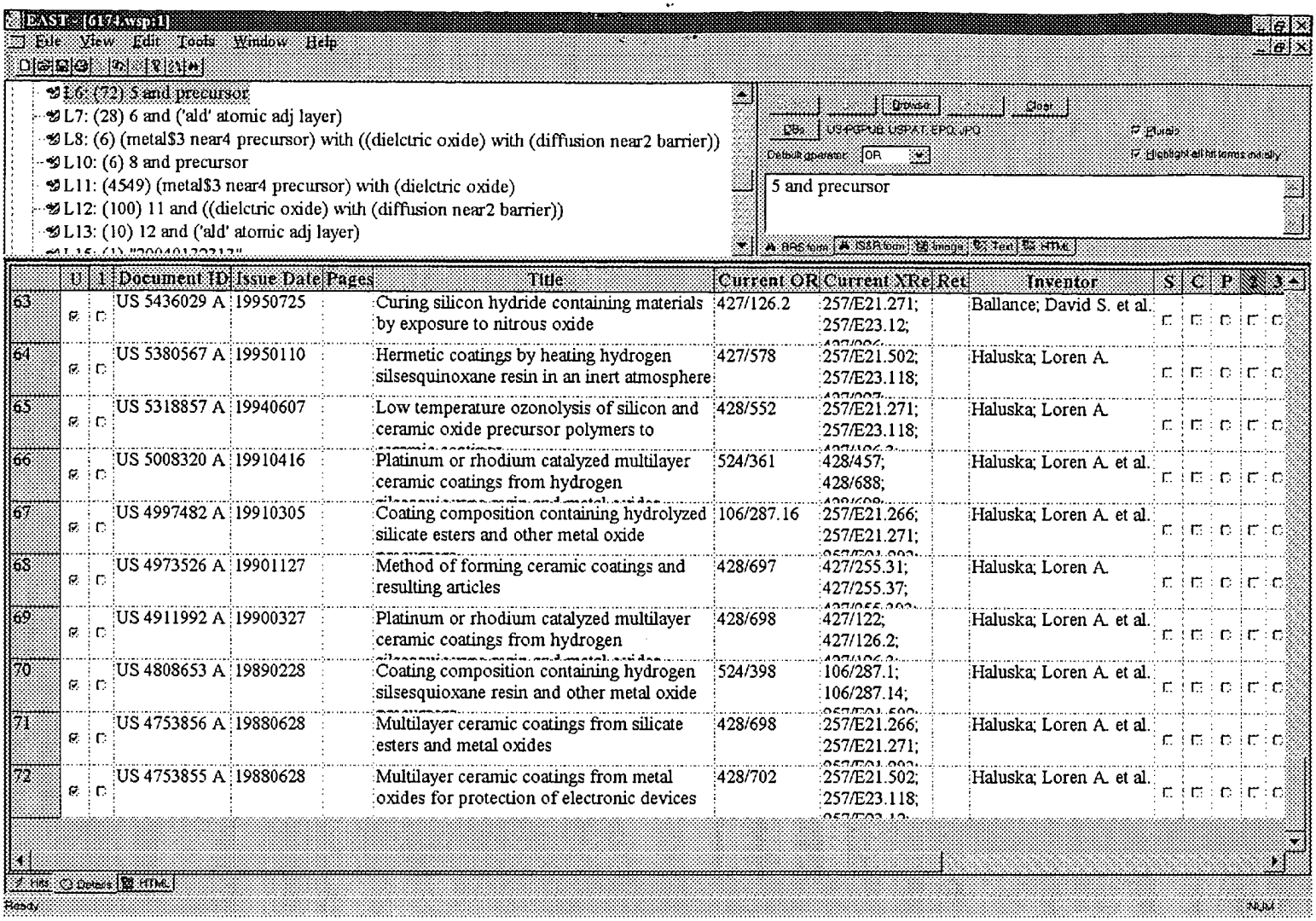
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63 US 5436029 A 19950725 Curing silicon hydride containing materials by exposure to nitrous oxide 427/126.2 257/E21.271; 257/E23.12; Ballance; David S. et al.
64 US 5380567 A 19950110 Hermetic coatings by heating hydrogen silsesquinoxane resin in an inert atmosphere 427/578 257/E21.502; 257/E23.118; Haluska; Loren A.
65 US 5318857 A 19940607 Low temperature ozonolysis of silicon and ceramic oxide precursor polymers to 428/552 257/E21.271; 257/E23.118; Haluska; Loren A.
66 US 5008320 A 19910416 Platinum or rhodium catalyzed multilayer ceramic coatings from hydrogen 524/361 428/457; 428/688; Haluska; Loren A. et al.
67 US 4997482 A 19910305 Coating composition containing hydrolyzed silicate esters and other metal oxide 106/287.16 257/E21.266; 257/E21.271; Haluska; Loren A. et al.
68 US 4973526 A 19901127 Method of forming ceramic coatings and resulting articles 428/697 427/255.31; 427/255.37; Haluska; Loren A.
69 US 4911992 A 19900327 Platinum or rhodium catalyzed multilayer ceramic coatings from hydrogen 428/698 427/122; 427/126.2; Haluska; Loren A. et al.
70 US 4808653 A 19890228 Coating composition containing hydrogen silsesquioxane resin and other metal oxide 524/398 106/287.1; 106/287.14; Haluska; Loren A. et al.
71 US 4753856 A 19880628 Multilayer ceramic coatings from silicate esters and metal oxides 428/698 257/E21.266; 257/E21.271; Haluska; Loren A. et al.
72 US 4753855 A 19880628 Multilayer ceramic coatings from metal oxides for protection of electronic devices 428/702 257/E21.502; 257/E23.118; Haluska; Loren A. et al.
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